(12) UK Patent Application (19) GB (11) 2 161 037 A

(43) Application published 2 Jan 1986

(21) Application No 8416556

(22) Date of filing 29 Jun 1984

(51) INT CL⁴
H02M 7/42 // 7/53

(52) Domestic classification
H2F 9K11 9K8 9L1 9M 9N1B2 9N2A 9N4A 9Q 9R20B 9R32C 9R39C 9R49B 9S2 9SX 9T5 TDA

(56) Documents cited
None

(58) Field of search
H2F

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(54) Inverter circuit arrangement

(57) An inverter comprises a pair of circuits (suffixed A and B respectively) each comprising a transformer 3 a primary winding 17 of which is connected with alternating polarity across input terminals 1, 2 via a choke 7 by means of a pair of switches 8, 9 (such as FET's Fig. 5) for periods equal to one-half the period of the resonant frequency of the resonant circuit comprising the transformer primary winding 17 and a capacitor 16 connected across it. The resonant frequency is the same for both circuits. To control the voltage across output terminals 4, 5 in spite of the constant-current properties of the chokes the transformers have a common secondary winding 18 and the phase of the antiphase switching signals applied to the switches of one circuit is made variable with respect to the phase of the antiphase switching signals applied to the switches of the other circuit by varying a control signal 13 applied to a switching signal generator 12, thereby varying the relative phases of the signals (V1, V2 Figs. 2a, 2b, 2c) contributing to the voltage (44, 37, 40) across the secondary winding. The transformers may have completely separate magnetic circuits or their magnetic circuits may have a portion in common, on which portion the secondary winding is provided.

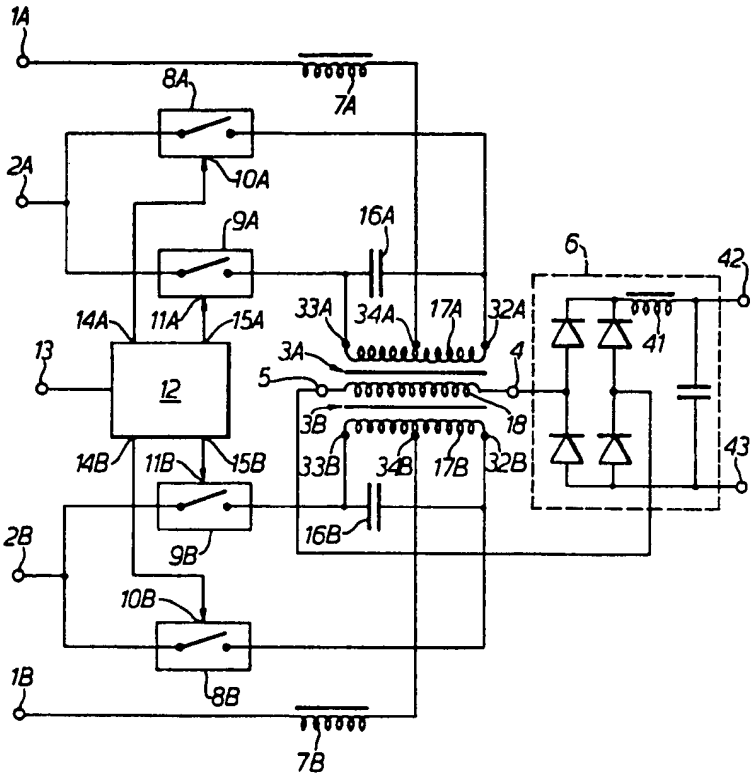

Fig.1.

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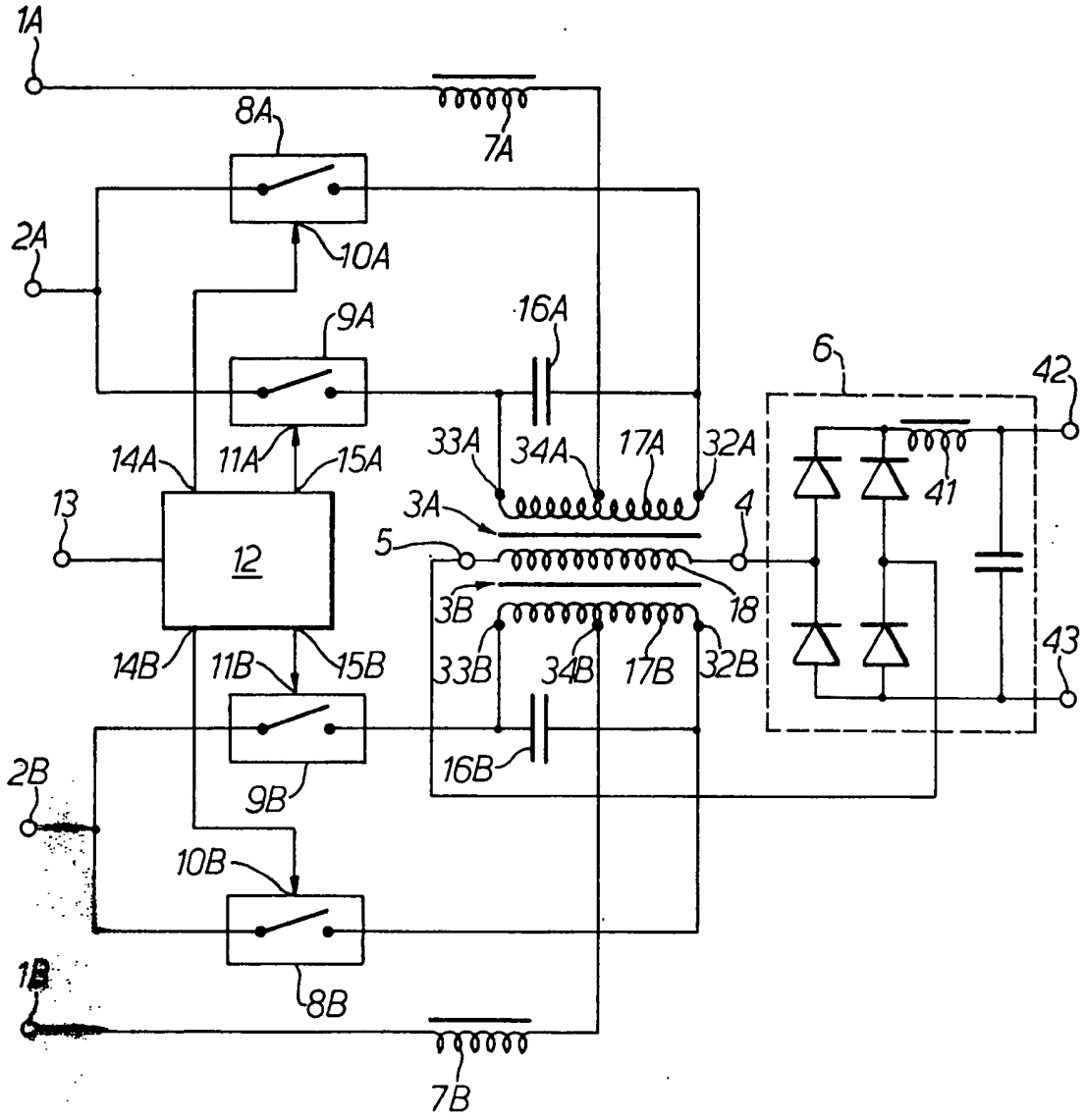

Fig.1.

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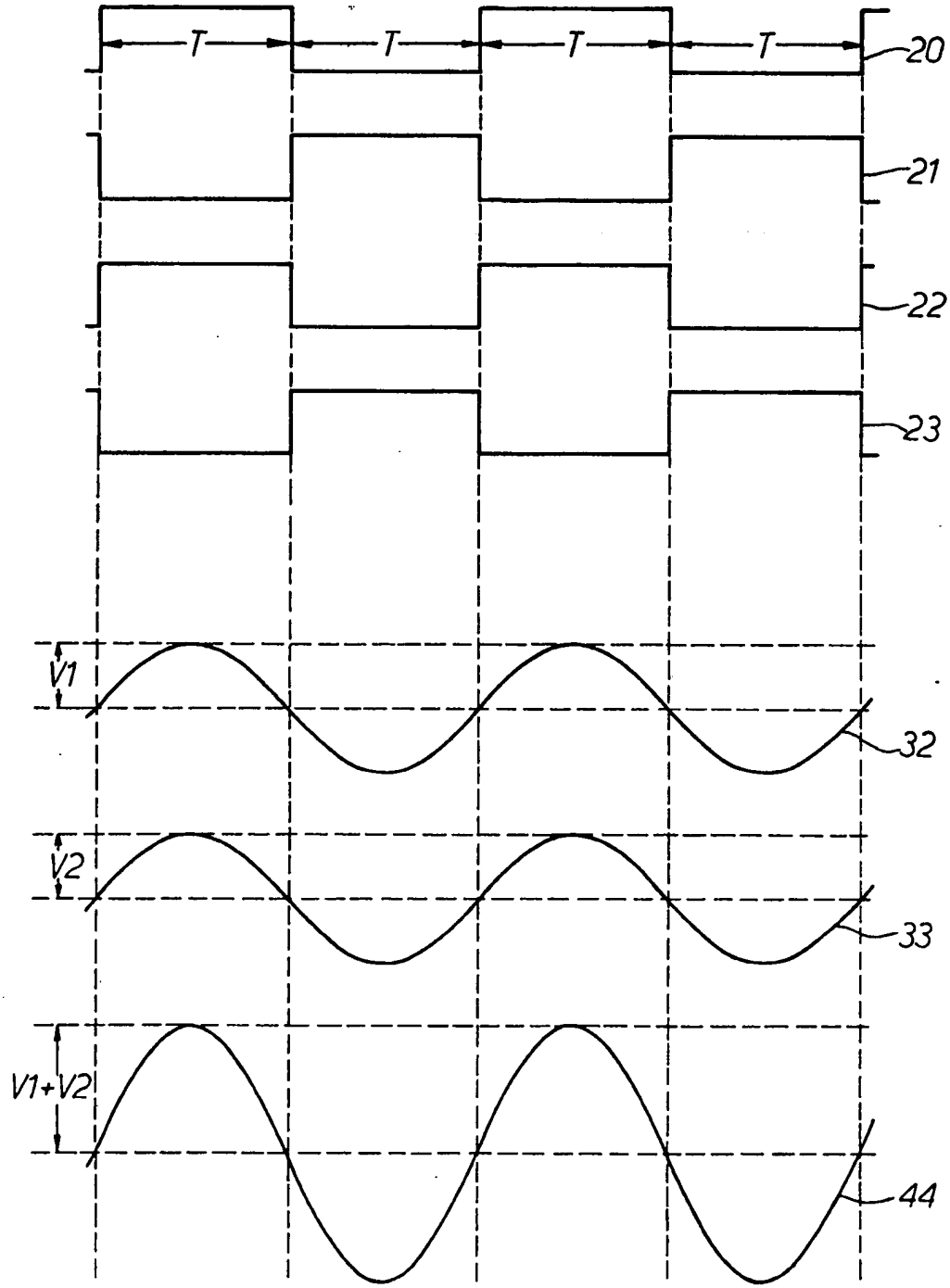

Fig. 2a.

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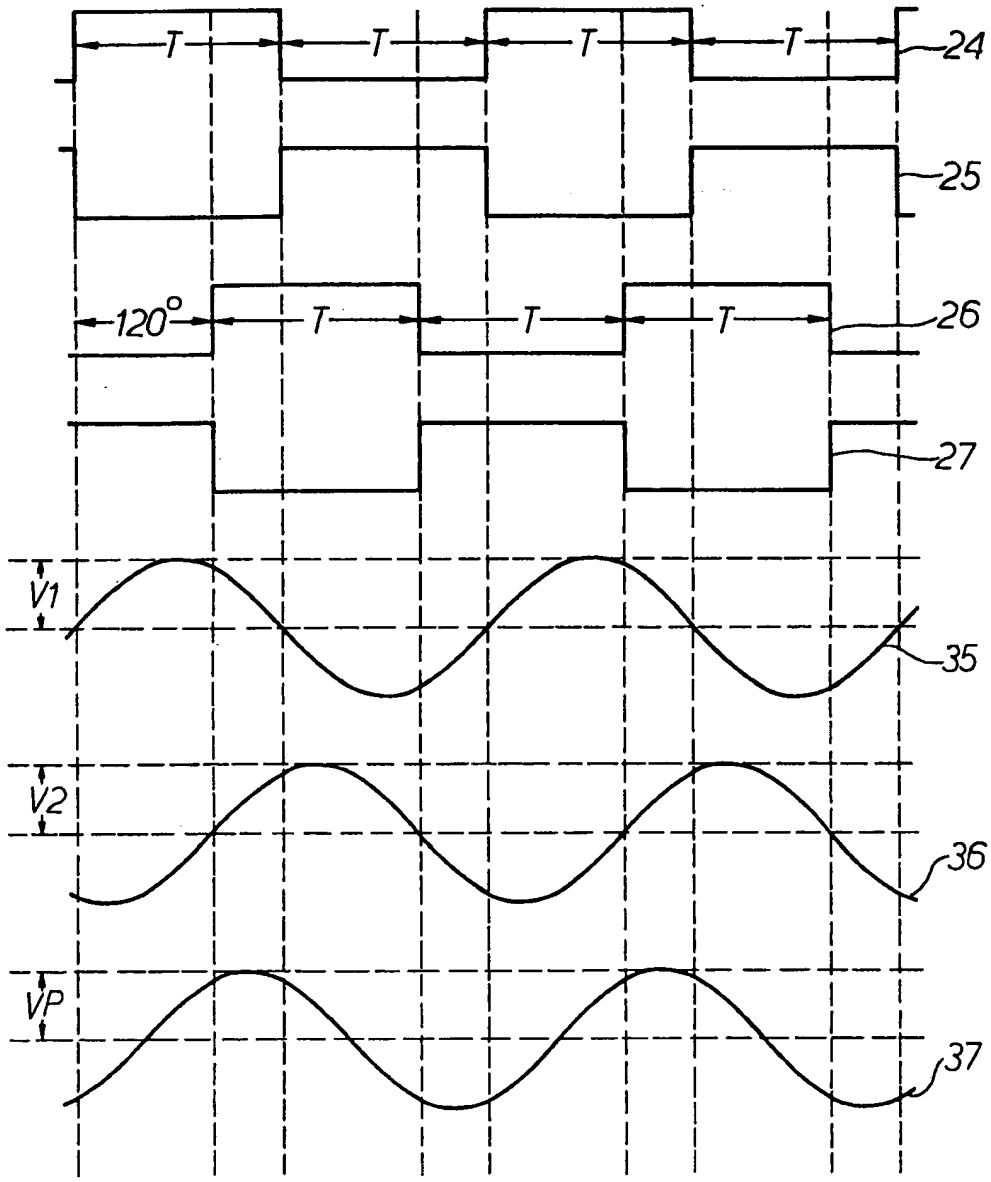

Fig. 2b.

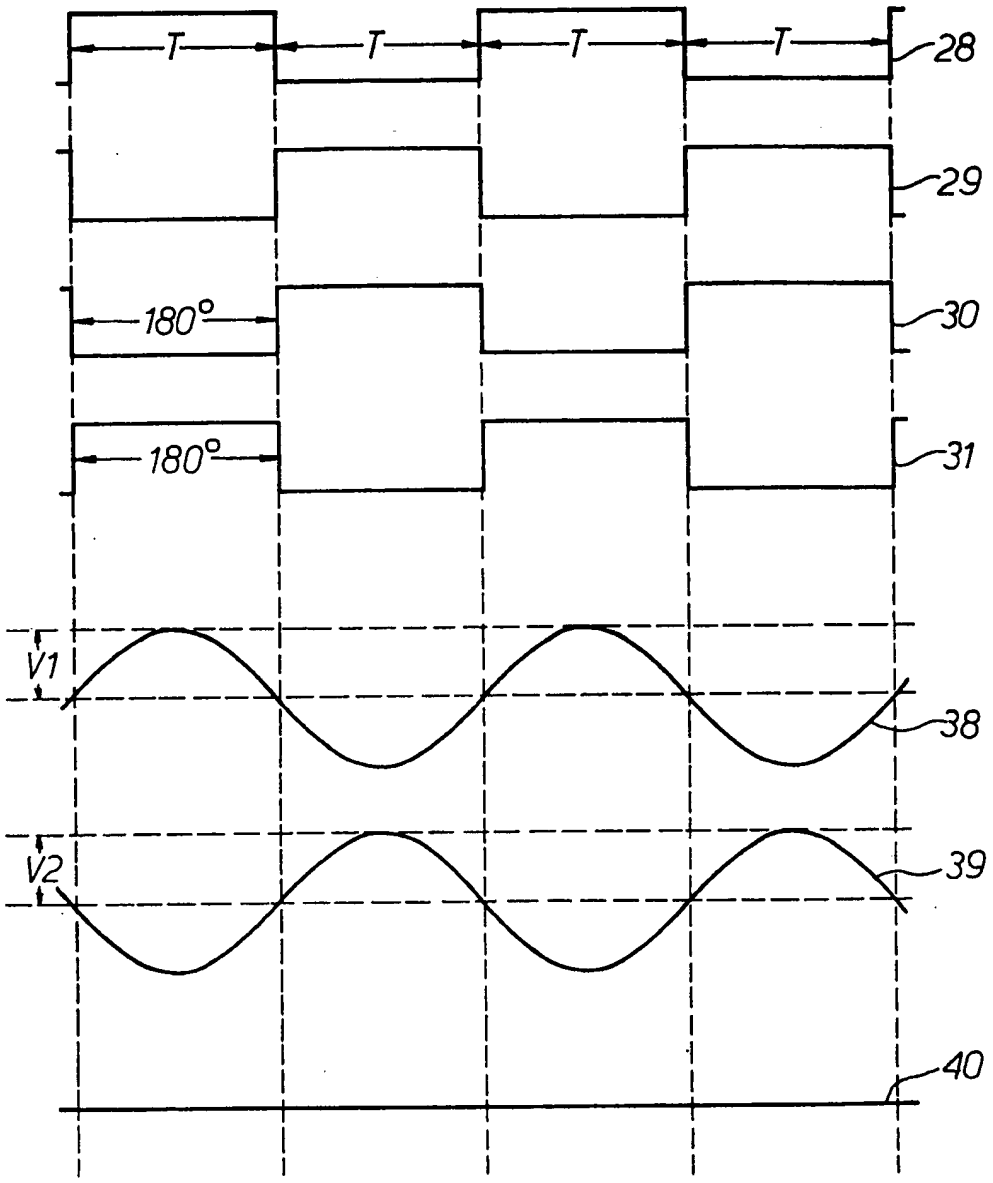

Fig. 2c.

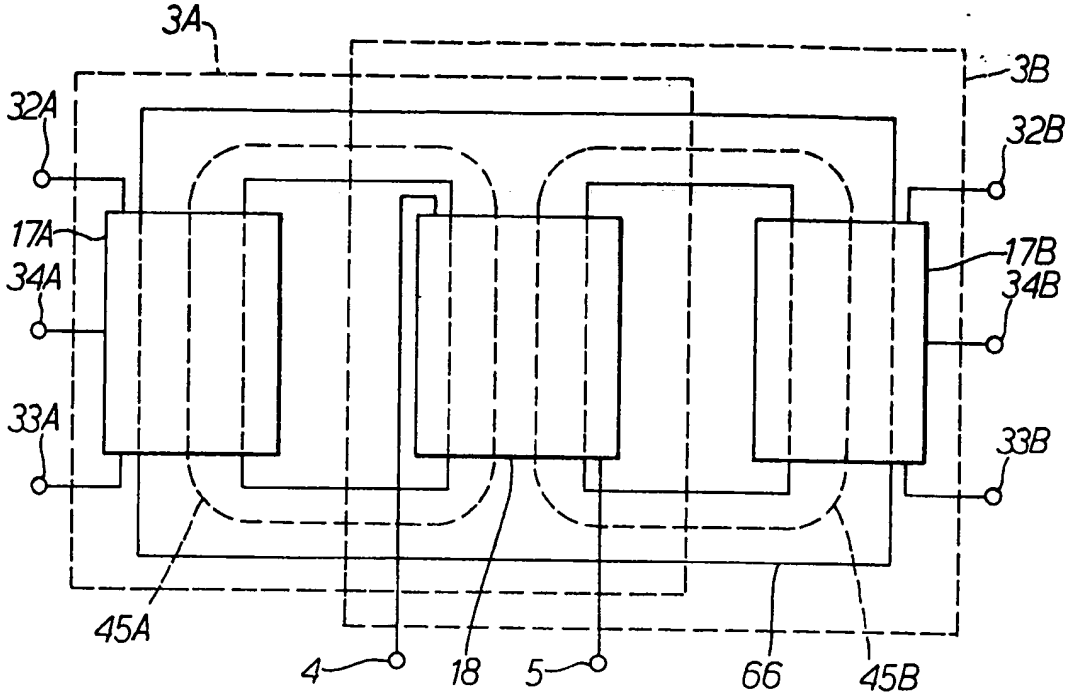

Fig.3.

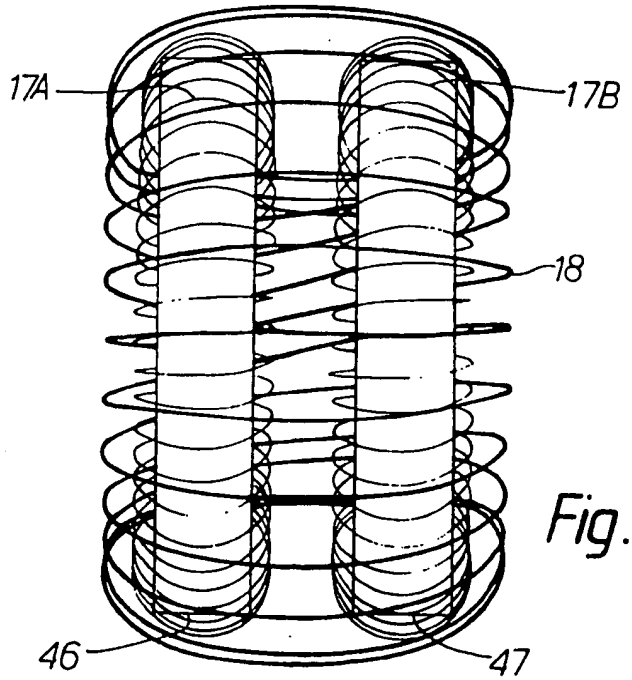

Fig.4.

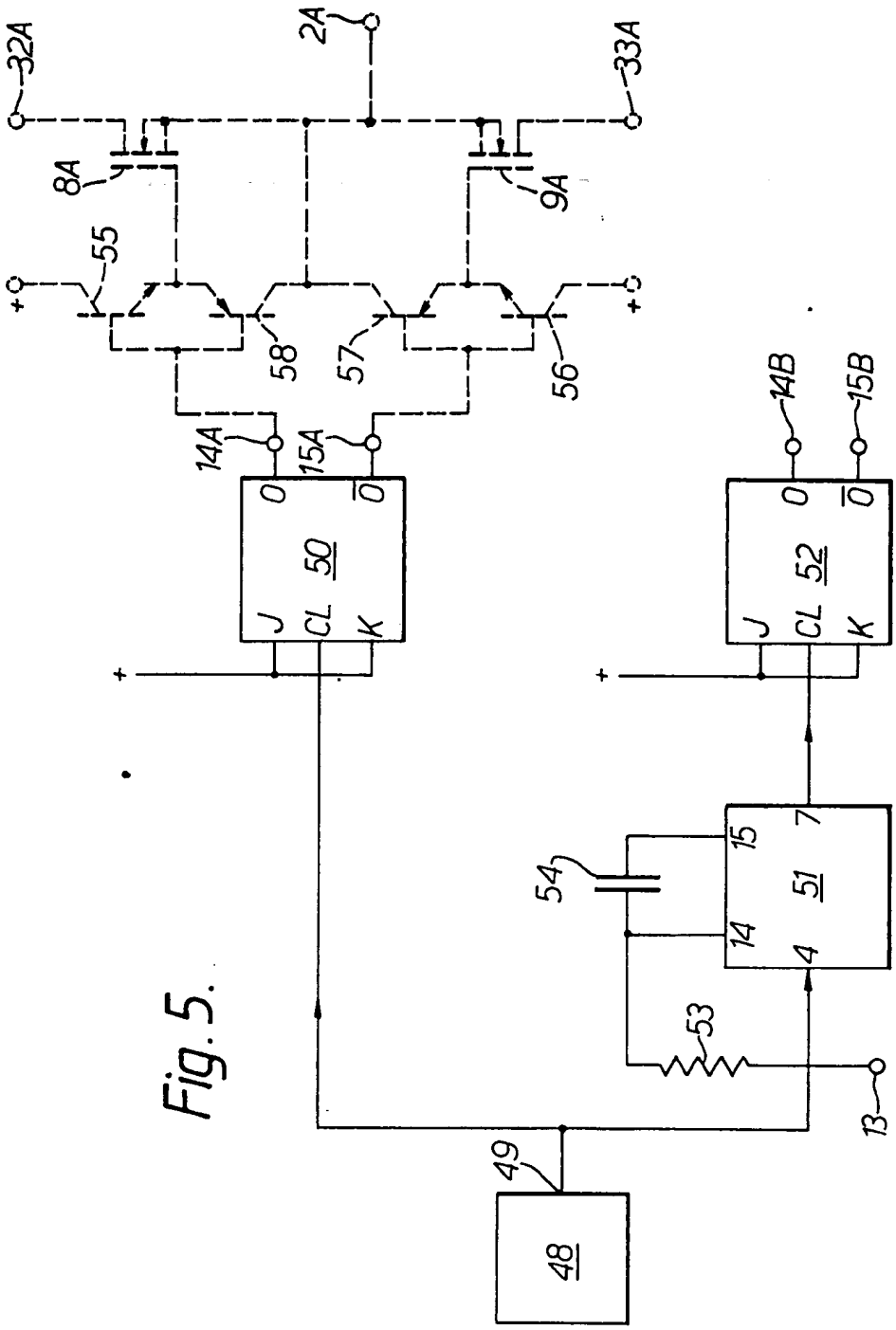

Fig. 5.

SPECIFICATION

Inverter circuit arrangement

This invention relates to an inverter circuit arrangement comprising a pair of d.c. input terminals, a transformer, a pair of output terminals to which a secondary winding of said transformer is coupled, first and second controllable switches which are each connected to form a series combination with a choke and at least part of a primary winding of said transformer in respective circuits which extend between said input terminals in such a sense that, when a d.c. voltage with a given polarity is applied between said input terminals and a given said switch is caused to conduct, a voltage will be set up across said secondary winding with the opposite polarity to that set up thereacross when the other said switch is caused to conduct, and a switching signal generator circuit which has a control input and is constructed to produce switch control signals at first and second outputs thereof, said first and second outputs being coupled to control inputs of said first and second switches respectively and said switch control signals being such as to render said switches conductive alternately. Such an arrangement will be referred to hereinafter as "an arrangement of the kind set forth".

A known arrangement of the kind set forth is discussed in the book "Design of solid-state power supplies" by E.R. Hnatek (2nd edition) pages 466-477. In this known arrangement the transformer has a primary winding to the two ends of which one of the input terminals is connected via respective ones of the (semiconductor) switches and to a centre-tap on which the other input terminal is connected via the choke, and a secondary winding which is connected to the output terminals and which also has a capacitor connected across it. The capacitor and the transformer secondary winding inductance together form a resonant circuit which is reflected to the primary side and is hence "seen" by the switches. (The capacitor could equally well be connected across the primary, or even be omitted altogether if parasitic capacitance inevitably present has an appropriate value). The conductive states of each switch recur at a rate substantially equal to the resonant frequency of the resonant circuit seen by the switches, and this fact in conjunction with the constant-current property of the choke results in the resonant circuit ringing at its natural frequency and, ideally, a sine-wave appearing at the output terminals (and across the primary winding). This can be a useful feature as it is likely to result in the generation of much less electromagnetic interference than is liable to be produced by inverters employing square wave voltages.

Because of the presence of the choke, however, it is rather difficult to regulate the output voltage of such an arrangement, at least by the conventional method of adjusting the ratio of the "closed" time to the "open" time of each of the two switches between a minimum of 0:1 and a maximum of 1:1; if this ratio is less than 1:1 both switches will repeatedly be open at the same time, resulting in the generation of very high voltages at the transformer end of the choke each time this occurs. In order to overcome this difficulty an auxiliary winding is provided on the choke in the known arrangement, this winding being connected across the input terminals via a diode which is poled to block the passage through it of current from the input terminals. The connection sense of the auxiliary winding is such that the voltage set up across this winding when current is being supplied to the transformer from the input terminals through the choke increases the reverse bias already present on the diode. However, when both switches are non-conductive this voltage changes sign, the diode in consequence conducts, and the energy stored in the choke is returned to the input supply through it, so that the aforesaid very high voltages no longer occur. Unfortunately, the fact that the supply of current to the transformer is still periodically broken means that spikes occur in the output voltage. Moreover, very rapid changes still occur in the overall potential of the primary winding. Both of these features are liable to appreciably degrade the otherwise low interference generation properties of the arrangement, and it is an object of the invention to mitigate this disadvantage.

The invention provides an inverter circuit arrangement of the kind set forth in the opening paragraph which is characterized in that said switch control signals are such as to render said switches conductive alternately for periods the durations of which are substantially equal to one-half the period of the resonant frequency of the resonant circuit including the transformer seen by said switches, in that said secondary winding is common to both said transformer and a second transformer also included in the arrangement, in that the arrangement includes third and fourth controllable switches which are each connected to form a series combination with a further choke and at least part of a primary winding of said second transformer in respective circuits which extend between a pair of d.c. input terminals in such a sense that, when a d.c. voltage with a given polarity is applied between these input terminals and a given one of said third and fourth switches is caused to conduct, a voltage will be set up across said secondary winding with the opposite polarity to that set up thereacross when the other one of said third and fourth switches is caused to conduct, in that said switching signal generator circuit is constructed to also

produce further switch control signals at third and fourth outputs thereof, said third and fourth outputs being coupled to control inputs of said third and fourth switches respectively and said further switch control signals being such as to render said third and fourth switches conductive alternately for periods the durations of which are substantially equal to one-half the period of the resonant frequency of the resonant circuit including the second transformer seen by said third and fourth switches, in that both said resonant frequencies are substantially the same, and in that said switching signal generator circuit is constructed to produce the further switch control signals at its third and fourth outputs with a predetermined phase relationship to the switch control signals produced at its first and second outputs, which phase relationship is dependent on the value of a control signal applied to the generator circuit control input.

It has now been recognized that providing, in effect, two arrangements of the kind set forth in the opening paragraph and effectively adding together the output waveforms of the two makes it possible to regulate the amplitude of the resulting waveform by varying the relative phases of the two waveforms which are effectively added together (assuming that their frequencies are the same), that the relative phases of the two waveforms can be varied by employing a switching signal generator circuit which generates switching signals for the third and fourth switches with phases which are controllable relative to the phases of the switching signals for the first and second switches, and that the two waveforms can be effectively added together by providing the two transformers with a common secondary winding. Two transformers having a common secondary winding can be a more compact component than, for example, two completely separate transformers having their secondary windings connected in series.

The magnetic circuits of the said transformers may simply have a portion in common, on which portion is provided said secondary winding. Thus, for example, the secondary winding may be provided on the centre limb of an "E-core" on the two outer limbs of which are provided the primary windings of the respective transformers. However this is liable to result in the length of the path of the flux generated by energisation of the primary windings changing with changes in the phase relationship between the waveforms in the two primary windings. As an alternative, therefore, the primary windings of said transformers may be constituted by respective members of a pair of mutually adjacent substantially coaxial toroidal winding s around separate respective ring-shaped cores, said secondary winding being around the toroidal windings collectively. As is known, toroidal windings need give rise to very little interaction with adjacent windings.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying diagrammatic drawings in which

Fig. 1 is the circuit diagram, partly in block-schematic form, of a first embodiment,

Figs. 2(a), 2(b) and 2(c) show some idealised waveforms illustrating the operation of the embodiment of Fig. 1,

Fig. 3 shows a first possible construction for part of the embodiment of Fig. 1,

Fig. 4 shows a second possible construction for part of the embodiment of Fig. 1 and

Fig. 5 is the circuit diagram of a possible construction for one of the blocks in Fig. 1.

In Fig. 1 an inverter circuit arrangement comprises a pair of d.c. input terminals 1A, 2A, a transformer 3A, a pair of output terminals 4, 5 to which a secondary winding 18 of transformer 3A is coupled, first and second controllable switches 8A and 9A respectively which are each connected to form a series combination with a choke 7A and part of a primary winding 17A of transformer 3A in respective circuits which extend between the input terminals 1A and 2A, and a switching signal generator circuit 12 which has a control signal input 13 and first and second outputs 14A and 15A respectively which are connected to control signal inputs 10A and 11A of switches 8A and 9A respectively. A capacitor 16A is connected between the ends 32A and 33A of primary winding 17A. The choke 7A connects input terminal 1A to a centre tap 34A on the primary winding 17A and, when conductive, the switches 8A and 9A connect input terminal 2A to the ends 32A and 33A respectively of the primary winding 17A. It will be noted that when a d.c. voltage of a given polarity is applied between input terminals 1A and 2A and, for example, switch 8A is caused to conduct, a current will flow through the series combination of switch 8A, choke 7A and the relevant half of the winding 17A in such a sense that the resulting voltage produced across winding 18 (and winding 17A) will be of the opposite polarity to that set up thereacross when switch 9A is caused to conduct and current flows through the series combination of switch 9A, choke 7A and the other half of primary winding 17A.

The arrangement also includes items 1B, 2B, 3B, 7B, 8B, 9B, 16B, 17B, 32B and 33B which are duplicates of, and interconnected in the same way as, the items 1A, 2A, 3A, 7A, 8A, 9A, 16A, 17A, 32A and 33A respectively. Winding 17B is the primary winding of the transformer 3B which has as its secondary winding the secondary winding 18 so that the output waveforms of transformers 3A and 3B are effectively added together in this common secondary winding, the result appearing across at the output terminals 4 and 5. The control inputs 10B and 11B of the switches

8B and 9B respectively are fed from third and fourth outputs 14B and 15B respectively of switching signal generator circuit 12. The input terminals 1B and 2B may, if desired, be common with respective ones of the input terminals 1A and 2A.

Switching signal generator 12 produces switch control signals at its outputs 14A, 15A, 14B and 15B, examples of which signals are illustrated at 20, 21, 22 and 23 respectively in the time diagrams of Fig. 2(a), 24, 25, 26 and 27 respectively in the time diagrams of Fig. 2(b), and 28, 29, 30 and 31 respectively in the time diagrams of Fig. 2(c), respectively, "high" levels of each signal corresponding to a closed or conductive state of the relevant switch and "low" levels of each signal corresponding to an open or non-conductive state of the relevant switch. The diagrams of Figs. 2(a), 2(b) and 2(c) relate to different values of a control signal applied to generator control input 13 in Fig. 1. It will be seen from these Figures that the switching signals are always such that the switches 8A and 9A conduct alternately, as do the switches 8B and 9B, and that the conduction periods of all the switches are of the same duration (T). However the phases of the conduction times of the switches 8A and 9A are variable relative to those of the conduction times of switches 8B and 9B by means of the control signal at input 13. The duration T is arranged to be substantially equal to one-half the period of the resonant frequency of the resonant circuit including the transformer 3A of Fig. 1 "seen" by the switches 8A and 9A, which resonant frequency is arranged to be itself substantially equal to the resonant frequency of the resonant circuit including the transformer 3B "seen" by the switches 8B and 9B (which is preferably done by making items 3A and 16A identical to items 3B and 16B respectively). These resonant circuits will, in the circuit of Fig. 1, consist in the main of the inductance of primary winding 17A in parallel with capacitor 16A, and the inductance of primary winding 17B in parallel with capacitor 16B respectively, although the resonant frequencies thereof will also depend somewhat upon the load supplied by secondary winding 18.

In the example of Fig. 2(a) the switching signals 20 and 22 are in phase with each other, as are the switching signals 21 and 23. As a result the sinusoidal contributions to the waveform appearing across secondary winding 18 due to the waveforms in primary windings 17A and 17B respectively are also in phase with each other (or in antiphase depending on the sense of connection of these primary windings and on the relative polarities of the d.c. supplies fed to the terminals 1A and 2A, and 1B and 2B); on the assumption that the former is the case they will be, for example, as shown at 32 and 33 respectively in Fig. 2(a). The peak values V1 and V2 are determined by the supply voltages between the terminals 1A and 2A, and between the terminals 1B and 2B, respectively and by the winding turns ratio in the transformer 3A and in the transformer 3B respectively. The sinusoidal waveform appearing across output terminals 4 and 5, being the sum of the contributions 32 and 33, is therefore as shown at 44 in Fig. 2(a); it has a peak value of (V1 + V2).

The waveforms 24, 25, 26, 27, 35, 36 and 37 in Fig. 2(b) correspond to the waveforms 20, 21, 22, 23, 32, 33 and 44 in Fig. 2(a). Again the switching signals are such that switches 8A and 9A conduct alternately for periods of duration T (signals 24 and 25) and switches 8B and 9B conduct alternately also for periods of duration T (signals 26 and 27), but now the control signal applied to generator control input 13 is such that the phases of the switching signals for switches 8B and 9B lag those of the switching signals for switches 8A and 9A by 120°, producing a corresponding lag in the output contribution 36 due to the waveform in winding 17B relative to the output contribution 35 due to the waveform in winding 17A. The result is that the peak value VP of the sum waveform 37 across output terminals 4 and 5 is considerably reduced. If, for example, $V1 = V2 = V$ say, it is equal to V, as opposed to 2V in Fig. 2(a).

The waveforms 28, 29, 30, 31, 38, 39 and 40 in Fig. 2(c) correspond to the waveforms 20, 21, 22, 23, 32, 33 and 44 in Fig. 2(a). Again the switching signals are such that switches 8A and 9A conduct alternately for periods of duration T (signals 28 and 29) and switches 8B and 9B conduct alternately also for periods of duration T (signals 30 and 31), but now the control signal applied to generator control input 13 is such that the phases of the switching signals for switches 8B and 9B lag those of the switching signals for switches 8A and 9A by 180°, producing a corresponding lag in the output contribution 39 due to the waveform in winding 17B relative to the output contribution 38 due to the waveform in winding 17A. The result is that the peak value of the sum waveform 40 across output terminals 4 and 5 is reduced even further; it is now $V1 - V2$, and for the purpose of Fig. 2(c) it has been assumed that $VI = V2$ so that the amplitude of the sum waveform 40 is zero.

Referring once again to Fig. 1 a mean-value rectifier circuit 6, i.e. a rectifier circuit including a series inductance or choke 41, may be connected to the output terminals 4 and 5 so that the overall circuit arrangement becomes a d.c.-d.c. converter circuit arrangement having output terminals 42 and 43. As shown the rectifier circuit is of the full-wave type but it will be appreciated that it may alternatively be of the half-wave type.

It will be evident that the arrangement of Fig. 1 may be modified by transferring the chokes 7A and 7B, the inductances of which are preferably at least five times that of one half of the primary winding 17A and one-half of the primary winding 17B respectively, to positions in the common connections from input terminal 2A to the switches 8A and 9A and from input terminal 2B to the switches 8B and 9B respectively, or the requisite inductances may be distributed between the positions shown and these other positions. If the resonant frequency of the resonant circuit including transformer 3A "seen" by switches 8A and 9A, and the resonant frequency of the resonant circuit including transformer 3B "seen" by switches 8B and 9B are required to be, for example, approximately 50 kHz, the inductance of one-half of each of the primary windings 17A and 17B may be arranged to be approximately 125 μH (inductance of each complete primary winding 500 μH) and the capacitances of the capacitors 16A and 16B may be approximately 20 nF. With these values the inductances of the chokes 7A and 7B may each be approximately 700 μH. It will also be evident that the capacitors 16A and 16B may each be replaced by a pair of capacitors, one capacitor being connected across each of the switches 8A, 9A, 8B and 9B, or be omitted altogether if the parasitic capacitance inevitably present has an appropriate value. If desired, the two halves of each primary winding 17A and 17B may be replaced by two completely separate (but interconnected) windings.

Another possible modification to the arrangement of Fig. 1 is to dispense with the centre-taps 34A and 34B, connecting the right-hand ends of the chokes 7A and 7B instead to the winding ends 32A and 32B respectively and providing two further chokes identical to the chokes 7A and 7B respectively and connected between input terminal 1A and winding end 33A, and between input terminal 1B and winding end 33B respectively.

The switching signal generator 12 (a possible construction for which will be described below with reference to Fig. 5) may be self-oscillating (in which case the correct time relationships between the switching signal pulses at its outputs will all have to be determined by suitably chosen internal time constants in conjunction with the control signal applied to its control input 13) or be provided with a feedback signal path from at least one of the transformers 3A and 3B. The control signal applied to its control input 13 may, if desired, be in the form of an error signal derived in a manner known per se by comparing a voltage derived from the output terminals 42 and 43 with a reference voltage.

One possible way of constructing the transformers 3A and 3B of Fig. 1 is illustrated in outline in Fig. 3, in which components having counterparts in Fig. 1 have been given the same references. In Fig. 3 the magnetic circuits of the transformers 3A and 3B, indicated by dashed lines 45A and 45B respectively, both run through a single block 66 of soft-magnetic material which is shaped to form a centre core for the common secondary winding 18 and, on either side of this centre core, cores for the primary windings 17A and 17B respectively, each end of each core being joined to the corresponding end of the other two cores. Thus the magnetic circuits 45A and 45B have a portion in common (that constituted by the centre core) on which portion the common secondary winding 18 is provided. If, say, the relative phases of the voltages across the primary windings 17A and 17B are such that the resulting fluxes in the magnetic circuits 45A and 45B flow one in a clockwise direction and one in an anti-clockwise direction as seen in the drawing, these fluxes will reinforce each other in the centre pole and hence in the secondary winding 18. Conversely, if the phases of the voltages across the primary windings 17A and 17B are such that the resulting fluxes in the magnetic circuits 45A and 45B both flow in a clockwise or an anticlockwise direction these fluxes will oppose each other in the centre pole and hence in the secondary winding 18. In fact in the latter case both fluxes will tend to flow instead around the overall periphery of the block 66, which means that the flux path lengths tend to vary with varying relative phases of the voltages across the two primary windings. Such varying flux path lengths mean that the effective inductances of the primary windings 17A and 17B also vary, which can be a nuisance as it means that the resonant frequencies of the corresponding resonant circuits including the capacitors 16A and 16B will themselves vary, causing difficulties in the design of the switching signal generator circuit 12. However, the construction of Fig. 3 does have the advantage of simplicity.

A way of overcoming the problem of changing effective inductance of the primary windings 17A and 17B in Fig. 3 is to employ a toroidal construction for each, as shown in the very schematic side-view of Fig. 4. As is known, toroidal windings need give rise to very little interaction with adjacent windings and, in Fig. 4, the toroidal windings 17A and 17B, each around a separate respective ring-shaped core (46 and 47 respectively), are substantially coaxial and are mounted side-by-side adjacent each other. This enables the common secondary winding 18, which is itself toroidal, to be provided around them collectively as shown.

Fig. 5 is the circuit diagram of a possible construction for the switching signal generator 12 of Fig. 1. It comprises an astable multivibrator 48, for example an integrated circuit

available under the type number HEF 4047, provided with appropriate timing components to ensure that the frequency of its output pulses is substantially equal to twice the resonant frequency of the resonant circuit including transformer 3A "seen" by switches 8A and 9A, and also substantially equal to twice the resonant frequency of the resonant circuit including transformer 3B "seen" by switches 8B and 9B. The output 49 of multivibrator 48 is connected to the clock signal input CL of a J-K flip-flop 50, for example half an integrated circuit available under the type number HEF 4027, both the J and K inputs of which are held at a high level so that it operates as a (positive edge triggered) frequency divider-by-two. The inverting and non-inverting outputs of this flip-flop constitute respective ones of the outputs 14A and 15A in Fig. 1. The output 49 of multivibrator 48 is also connected to the (positive edge responsive) trigger input of a monostable multivibrator 51, in the present example pin 4 of an integrated circuit available under the type number HEF 4528. Pin 7 of this integrated circuit, at which a negatively-directed pulse appears when the monostable is triggered, is connected to the clock input of a J-K flip-flop 52, for example the other half of the aforesaid integrated circuit HEF 4027. Like flip-flop 50, the J and K inputs of flip-flop 52 are held at a high potential, so that this flip-flop too acts as a positive edge triggered frequency divider-by-two. The inverting and non-inverting outputs of this flip-flop constitute respective ones of the outputs 14B and 15B in Fig. 1. The durations of the unstable states of multivibrator 51 are controllable by means of the control signal applied to control input 13. To this end input 13 is connected to pin 14 of the integrated circuit via a timing resistor 53, this pin being connected in turn to pin 15 via a timing capacitor 54. The values of this capacitor and resistor are chosen so that when the voltage on control input 13 is comparatively high, for example + 10V, the durations of the unstable states of multivibrator 51 are negligible compared with half the period of the output pulses of multivibrator 48, whereas as the value of the control signal at input 13 is reduced these durations increase to a maximum of, for example, half the said period. Thus the instants at which (positive going) trailing edges occur at the output of multivibrator 51, and hence at the clock input of flip-flop 52, can be continuously varied between substantial coincidence with the occurrence of the positive-going edges at output 49 of multivibrator 48 (and hence at the clock input of flip-flop 50) and, for example, substantial coincidence with the immediately succeeding negative-going edges at output 49.

The switches 8A, 9A, 8B and 9B of Fig. 1 may be in the form of power MOSFETs, for example those available under the type number BUZ 80, in which case the outputs of the flip-flops 50 and 52 may be coupled to their control inputs or gates in the manner indicated in Fig. 5 in dashed lines for the outputs 14A and 15A and the corresponding switches 8A and 9A. The npn transistors 55 and 56 may be, for example, those available under the type number BC 337, and the pnp transistors 57 and 58 may be, for example, those available under the type number BC 327.

CLAIMS

1. An inverter circuit arrangement comprising a pair of d.c. input terminals, a transformer, a pair of output terminals to which a secondary winding of said transformer is coupled, first and second controllable switches which are each connected to form a series combination with a choke and at least part of a primary winding of said transformer in respective circuits which extend between said input terminals in such a sense that, when a d.c. voltage with a given polarity is applied between said input terminals and a given said switch is caused to conduct, a voltage will be set up across said secondary winding with the opposite polarity to that set up thereacross when the other said switch is caused to conduct, and a switching signal generator circuit which has a control input and is constructed to produce switch control signals at first and second outputs thereof, said first and second outputs being coupled to control inputs of said first and second switches respectively and said switch control signals being such as to render said switches conductive alternately, characterized in that said switch control signals are such as to render said switches conductive alternately for periods the durations of which are substantially equal to one-half the period of the resonant frequency of the resonant circuit including the transformer seen by said switches, in that said secondary winding is common to both said transformer and a second transformer also included in the arrangement, in that the arrangement includes third and fourth controllable switches which are each connected to form a series combination with a further choke and at least part of a primary winding of said second transformer in respective circuits which extend between a pair of d.c. input terminals in such a sense that, when a d. c. voltage with a given polarity is applied between these input terminals and a given one of said third and fourth switches is caused to conduct, a voltage will be set up across said secondary winding with the opposite polarity to that set up thereacross when the other one of said third and fourth switches is caused to conduct, in that said switching signal generator circuit is constructed to also produce further switch control signals at third and fourth outputs thereof, said third and fourth outputs being coupled to control inputs of said third and fourth swit-

ches respectively and said further switch control signals being such as to render said third and four th switches conductive alternately for periods the durations of which are substantially equal to one-half the period of the resonant frequency of the resonant circuit including the second transformer seen by said third and fourth switches, in that both said resonant frequencies are substantially the same, and in that said switching signal generator circuit is constructed to produce the further switch control signals at its third and fourth outputs with a predetermined phase relationship to the switch control signals produced at its first and second outputs, which phase relationship is dependent on the value of a control signal applied to the generator circuit control input.

2. An arrangement as claimed in Claim 1, characterized in that the magnetic circuits of the said transformers have a portion in common, on which portion is provided said secondary winding.

3. An arrangement as claimed in Claim 1, characterized in that the primary windings of said transformers are constituted by respective members of a pair of mutually adjacent substantially coaxial toroidal windings around separate respective ring-shaped cores, and in that said secondary winding is provided around the toroidal windings collectively.

4. A d.c.-d.c. converter circuit arrangement comprising an arrangement as claimed in any preceding claim and a mean-value rectifier circuit connected to said output terminals.

5. An inverter circuit arrangement substantially as described herein with reference to Fig. 1 of the drawings, Figs. 1 and 5 of the drawings, or to said Fig. 1 or Figs. 1 and 5 together with Fig. 3 or Fig. 4 of the drawings.

Printed in the United Kingdom for
Her Majesty's Stationery Office, Dd 8818935, 1986, 4235.
Published at The Patent Office, 25 Southampton Buildings,
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